Challenges in Manufacturing FinFET at 20nm node and beyond

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Abstract

Recently, there is strong interest in FinFET technology on bulk for lower cost and good compatibility with planar CMOS. Intel's 22nm CMOS node is the 1st commercially available bulk-FinFET technology and opens a new era of 3D CMOS for the low-power mobile electronics and continuously driving CMOS scaling and Moore's law. The challenges in manufacturing FinFETs are reviewed. The Si surface of fins appears different than in bulk and result in excessive Si loss in wet cleans, oxidation, and dry etching. The shape of active fins leads to preferred low-doping in channel for minimizing variations of Vt . Then, multi-Vcc scheme is used for SOC instead of the multi-Vt scheme (based on multiple work-function of gate). In order to prevent dopant diffusion into the channel, the fins are preferably formed on SOI or bulk substrate with super-steep retrograde well (SSRW) doping. Finally, the contact and gate metals provide new knobs (in addition to the usual stressor S/D epi) for strain engineering for FinFETs toward higher performance at lower Vcc and power.

Introduction

Recent Intel's progresses at 22nm node [1] not only shows the phasing out of the planar CMOS and the dawn of a 3D CMOS (FinFET) era, but also the start of the low-power for mobile electronics as a new driving force of device scaling and Moore's law. FinFET was originally developed on SOI, but recently, there is strong interest in forming FinFET on bulk (***Fig. 1***) for lower cost and better compatibility with planar CMOS. The process flow starts the fin formation similarly as the formation of active area (in planar CMOS) and followed by STI gap-fill and planarization and oxide recessing to reveal the fins. Then the rest of flow proceeds to similar steps (e.g. well, gate, epi-S/D, etc.) as the planar CMOS with gate-last high-k and metal-gate (HKMG) flow.

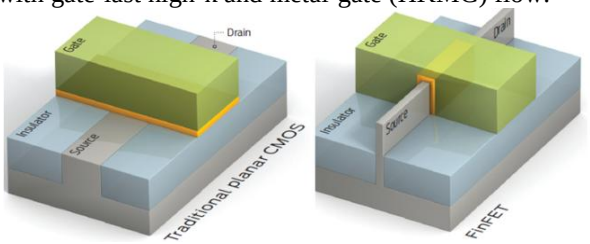

Fig. 1: The FinFET on bulk has good process compatibility to planar CMOS and leads to low cost [1].

Technology features and Process flow of FinFET

Technology of Intel's 22nm bulk-FinFET [2] is summarized here (***Fig. 2***). The contacted gate pitch is 90nm and the SRAM cell size is scaled to 0.092um2. The fin is thin (~8nm) with trapezoidal shape and fully-depleted channel for improved short-channel effects (SCE). The fin height (~35nm) is optimized for performance between the drive current and capacitance. To reduce the Rext for transistor performance, raised S/D (with in-situ doping) is used for n-FinFET. To induce compressive stress in channel, eSiGe (with ~55% Ge) of S/D is used for p-FinFET. The gate stack with high-k and metal-gate (HKMG) [3] is used in FinFET with careful optimization related to the corners and sidewall for good reliability. In BEOL, the self-aligned contact (SAC) process is enabled by recessing the W-gate metal and followed by a Si-nitride and oxide capping layers and CMP planarization prior to contact patterning. The contacts are etched selectively to the Si-nitride (for protecting the gates). There are 9 layers of Cu interconnect with low-k or ultra-low-k dielectric providing lower capacitance than 32nm node.

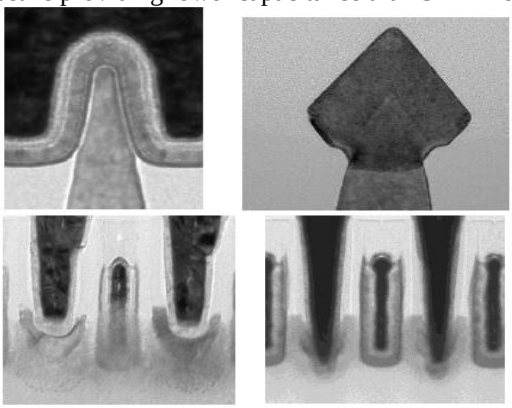

Fig. 2: The bulk-FinFET features small fins, gate-last HKMG, epi S/D for n and pMOS, self-aligned contact (SAC), and advanced BEOL [2].

Challenges in Manufacturing FinFETs

There are challenges of FinFET manufacturing as discussed recently [4], mainly in economics, lithography and double patterning, MOL and self-aligned contacts, severe layout dependent effects, and more DFM. In addition to these typical challenges above, there are a few new process and materials challenges in manufacturing FinFET as summarized below. ***Firstly***, the Si surface of fins appears different

than in bulk, so that excessive Si loss was observed after the usual pre-gate-oxide clean (***Fig. 3a***). Thus wet cleans are optimized with dilute concentration and lower temperatures. Similarly, the oxidation of fin is also faster at corner and tip of fins. Furthermore, the dry etching on fins is more stringent [5] due to the 3D structures (***Fig. 3b***) and a bias plasma pulsing scheme may be viable for minimizing Si loss. ***Secondly***, as a result of the shape of active fins, the fin channel is preferred to be low-doping for minimizing Vt variations related to random doping fluctuations (RDF). As the Vt of low-doping channel is mainly set by the work-function of gate electrode, it leads to difficult and costly implementation of multi-Vt (by using multiple gate materials); fortunately, multi-Vcc scheme can be used for SOC applications (***Fig. 4***) [6]. ***Thirdly***, to prevent dopant diffusion into channel from the Halo implant at S/D, the FinFET can be formed on SOI or bulk with super-steep retrograde well (SSRW) doping (***Fig. 5***) [7]. ***Fourthly***, as the etch-stop liner is known not effective as stressor for FinFET, the non-merged and recessed fin before S/D epi provides effective stress to fin-channel. The contact and gate metals can provide new knobs of strain engineering for FinFETs [8-9] for higher performance at lower Vcc.

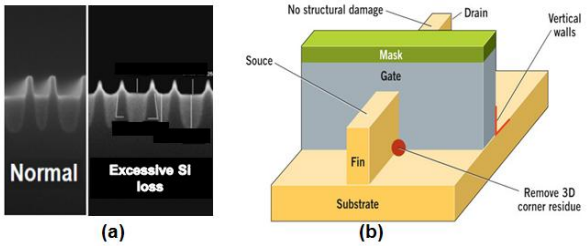

Fig. 3: (a) The Si-loss of fins appears more severe than bulk. (b) The plasma etching is more difficult on 3D structures [5].

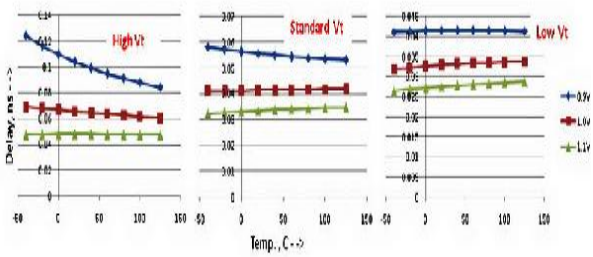

Fig. 4: By selecting standard-Vt and multiple Vcc, the circuit can cover good range in temperature-delay domain [6] for SOC applications.

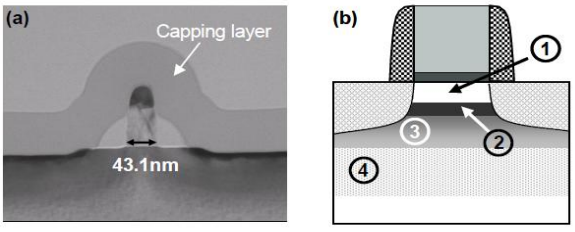

Fig. 5: Multiple layers are formed in p or n-well on bulk silicon substrate for SSRW substrate. Layer-1 is the low doped Si for active fin channel. Layer-2 and 3 are buffer layers (containing Carbon) for suppressing dopant diffusion from layer 4 (with higher doping in well to prevent sub-channel punch-through) [7].

Acknowledgement

Thanks for helpful discussions from many colleagues in GLOBALFOUNDRIES.

Conclusion

Technology of Intel's 22nm bulk-FinFET opens a new era of CMOS technology and continuously driving the future CMOS scaling toward low-power and Moore's law. We discuss challenges in manufacturing FinFET beyond those typical ones discussed in cost, lithography, MOL and self-aligned contacts, layout dependent effects, and DFM. ***Firstly***, the Si surface on fins appears different than in bulk as supported by observation of excessive Si loss in wet/dry etching, faster oxidation, etc. ***Secondly***, as a result of the fin shape, the low-doping in channel is preferred for minimizing Vt variations. It also leads to costly implementation of multiple work-functions of gate; fortunately, the multi-Vcc scheme can be used for SOC applications. ***Thirdly***, to prevent dopant diffusion into channel from the Halo implant at S/D, the fins are formed on SOI or bulk with super-steep retrograde well (SSRW) doping. ***Fourthly,*** the contact and gate metals provide new knobs (in addition to the S/D epi) of strain engineering for FinFETs toward higher performance at lower Vcc and power.

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